

## 1.1 1.3 GHZ , FRACTIONAL DELTA-SIGMA SYNTHESIZER USING FPGA

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This paper introduces a new method for implementation of Fractional-N Delta-Sigma synthesizers. In this method, the delta-sigma modulator has been implemented in a FPGA IC. FPGA ICs have programmable hardware ,so they can easily be used to implement and compare various structures .

First, the phase noise of a fractional-N synthesizer using n-order Delta-Sigma modulator to control the divide ratio is calculated and it is shown theoretically that as the order of modulator increases the low frequency phase noise decreases. Then three different structures of Delta-Sigma modulators including 1st order , 2nd order and Mash 1-1-1 are implemented in a 1.1-1.3 GHz fractional synthesizer. The channel spacing is selected as 250 KHz but any smaller value can be implemented easily. Measurements verify the theoretical concepts about the influence of the order of the structure on the synthesizer phase noise.

The experimental results are exhibited and summarized and these results confirm the theoretical results too. These practical measurements show, the use of high order modulators in fractional-N synthesizer can decreases low frequency phase noise down to 90 dBc/Hz in the offset frequency of 100 Hz from the carrier.

One advantage of this design is that structures that can be implemented and measured on this board are not limited to the above structures. Any kind of structure being used to control the divide ratio in a fractional synthesizer can be implemented and tested by this board, so one of the most important use of this board is to test new designed structures before implementing them in an IC package.

Another advantage of this design, if used as a common fractional synthesizer in a system, is its possibility to be updated to any new structure that may be introduced for fractional synthesizers in the future thanks to the on board programming of FPGA IC.

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