DESIGN OF A LOW-POWER WIDE-LOCKING-RANGE VOLTAGE-CONTROLLED OSCILLATOR FOR COUPLED OSCILLATOR ARRAYS

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Coupled oscillator arrays (COAs) have been introduced as a low cost method to achieve the appropriate phase shift for phased array applications. For many applications, including space deployment, power limitations are an important criterion. For good COA performance, it is important to fabricate individual oscillator cells with wide locking range. The design objective was to fabricate a three-element COA with S-band oscillators operating at 10mW input power and a $\pm 5\%$ inter-element locking range.

The design process involved choosing an appropriate transistor and oscillator structure, optimizing the design for wide locking range, and verifying the requirements on tuning. In conventional oscillator design, it is desired in oscillator designs to have high-Q resonant structures to minimize the phase noise, but high-Q structures have a relatively small locking range. To achieve a large locking range, an oscillator requires a low-Q resonant structure. In the design process, this was accomplished by performing an optimization to minimize the slope of the phase of the oscillator open-loop gain.

The oscillator design included a varactor to achieve the desired tuning of the voltage controlled oscillator. After one iteration of the design, the value of capacitance was varied over the necessary range, and the oscillation frequency and phase slope were analyzed to verify that the oscillator still operated as desired. If the phase slope changed too drastically upon tuning, then the optimization was performed again with a new starting point.

After the circuit design met the desired specifications, a three-element array was fabricated. Each oscillator operated at a bias of 1.5V and about 5-6mA, which corresponds to 7.5-9.0mW of input power. Each oscillator also required a tuning voltage of 2-15V with current on the order of a few μA. The oscillators operated from 2.0-2.3GHz with an inter-element locking range measured as high as 5.2%.

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2. D - Electronics and Photonics

3. (a)

4. C - Contributed Paper

5. No special instructions