

COMPLEXITY REDUCTION VIA CONVERGENCE OF THE  
SUM-PRODUCT ALGORITHM FOR LDPC UNDER FADING  
CHANNELS

John,S.<sup>1,2</sup>, Kwon,H.M.<sup>1,3</sup>

<sup>1</sup>Wichita State University, 1845 Fairmount, Wichita, KS-67208

<sup>2</sup>Indian Institute of Technology of Kanpur, Kanpur, India.

<sup>3</sup>Senior Member IEEE

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LDPC codes are proved to approach near-Shannon limit of channel capacity when the length is long enough. It is desirable to have very long block length when the coding efficiency is concerned. Also thanks to the inherent interleaver effect, long codes are less likely to be completely corrupted in deep fades and can thus avoid serious performance degradation. However, the practical block length is confined by the implementation complexity of LDPC decoder, which increases significantly with block length. In this paper we show that for short length, less sparse parity matrices the decoding complexity is almost independent of noise statistics and number of iterations, (i.e. convergence is faster for the short length Low Density Parity Check Codes under the different fading channels as compare to the long length Low Density Parity Check Codes). Simulation results show that after certain number of iterations the decoding complexity becomes constant and the bit decision can be made under both, AWGN and Rayleigh fading channels. In this paper we reveal some efficient techniques to reduce the complexity of the Sum-Product algorithm for the Low Density Parity Check Code under the AWGN and Rayleigh Fading Channels to achieve approximately same bit error rate as proposed by the Belief Propagation Algorithm. Decoder convergence is utilized to reduce the processing time for the decoding of the bit under the AWGN and Rayleigh Fading channels. We also propose that how the complex computation can be confined to overcome the overflow and underflow at the message passing points, i.e. Bit node to Check node and Check node to Bit node propagation paths, via decomposing the complex matrix to the real matrix. The simulation results also reveal the convergence of likelihood surfaces at the Bit Node to Check Node and Check Node to Bit Node and how the extrinsic information is passed to decode the bit. We observe the three types of error that occur at the different SNRs and the decoder behavior is changing as the SNR changes, We also propose that these errors can also be corrected by simple procedures, and hence Maximum likelihood rule for decoding the bit can also be supported to reduce the error in bits according to the SNR values and the convergence graph of the respective bit. This algorithm can be implemented in chip designing with less complexity and via the structured programming.

1. (a) Sudhanshu John  
1742 N Yale  
Wichita, KS  
67208 USA  
sxjohn@wichita.edu
- (b) 3166841340
- (c)
2. E - Electromagnetic Noise  
and Interference
3. (a)
4. C - Contributed Paper
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