# SPECIFICATION CORRECTIONS FOR THE PCI-6110E/6111E

Appendix A, *Specifications*, in the *PCI-6110E/6111E User Manual*, contains incorrect information. Use the specifications below instead of those in your user manual.

These specifications listed in this document are typical at 25° C unless otherwise noted.

## Analog Input

### Input Characteristics

Number of channels

PCI-6110E .....4 differential

PCI-6111E .....2 differential

Resolution.....12 bits, 1 in 4,096

Max sampling rate .....5 MS/s

Min sampling rate .....1 kS/s

Input signal ranges

| **Channel Gain (Software-Selectable)** | **Input Ranges**[1] |
|---|---|
| 0.2 | ±50 V |
| 0.5 | ±20 V |
| 1 | ±10 V |
| 2 | ±5 V |
| 5 | ±2.0 V |



  

| Channel Gain (Software-Selectable) | Input Ranges[1] |
|---|---|
| 10 | ±1 V |
| 20 | ±500 mV |
| 50 | ±200 mV |

[1] **Warning:** The 611*X* E is not designed for input voltages greater than 42 V, even if a user-installed voltage divider reduces the voltage to within the input range of the DAQ device. Input voltages greater than 42 V can damage the 611*X* E, any device connected to it, and the host computer. Overvoltage can also cause an electric shock hazard for the operator. National Instruments is NOT liable for damage or injury resulting from such misuse.

Input coupling ..... DC/AC

Max working voltage

ACH<0..3>+ ..... Should remain within ±11 V (gain ≥ 1) ±42 V (gain <1)

ACH<0..3>– ..... Should remain within ±11 V

Overvoltage protection ..... ±42 V

Inputs protected ..... ACH<0..3> + ACH<0..3> –

FIFO buffer size ..... 8,192 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather

## Accuracy Information

See following table

# PCI-6110E/6111E Accuracy Information

| Nominal Range (V) | | Absolute Accuracy | | | | | | | Relative Accuracy | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | % of Reading | | | Offset | Noise + Quantization (mV) | | Temp Drift | Resolution (mV) | |
| Positive FS | Negative FS | 24 Hours | 90 Days | 1 Year | (mV) | Single Pt. | Averaged | (%/° C) | Theoretical | Averaged |
| 50 | –50 | 0.5071% | 0.5079% | 0.5088% | 34.669 mV | 50.732 mV | 4.395 mV | 0.0005% | 24.414 mV | 5.786 mV |
| 20 | –20 | 0.5071% | 0.5079% | 0.5088% | 19.387 mV | 20.293 mV | 1.758 mV | 0.0005% | 9.766 mV | 2.314 mV |
| 10 | –10 | 0.1071% | 0.1079% | 0.1088% | 5.738 mV | 10.146 mV | 0.879 mV | 0.0005% | 4.883 mV | 1.157 mV |
| 5 | –5 | 0.0571% | 0.0579% | 0.0588% | 2.971 mV | 5.073 mV | 0.439 mV | 0.0005% | 2.441 mV | 0.579 mV |
| 2 | –2 | 0.0571% | 0.0579% | 0.0588% | 1.272 mV | 2.029 mV | 0.176 mV | 0.0005% | 0.977 mV | 0.231 mV |
| 1 | –1 | 0.0571% | 0.0579% | 0.0588% | 0.698 mV | 1.015 mV | 0.088 mV | 0.0005% | 0.488 mV | 0.116 mV |
| 0.5 | –0.5 | 0.0571% | 0.0579% | 0.0588% | 0.402 mV | 0.669 mV | 0.059 mV | 0.0005% | 0.244 mV | 0.077 mV |
| 0.2 | –0.2 | 0.0571% | 0.0579% | 0.0588% | 0.204 mV | 0.390 mV | 0.035 mV | 0.0005% | 0.098 mV | 0.046 mV |

**Note:** Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.
Measurement accuracies are listed for operational temperatures within ±1° C of internal calibration temperature and ±10° C of external or factory calibration temperature.
One year calibration interval recommended.

## Transfer Characteristics

INL ..... ±0.5 LSB typ, ±1 LSB max

DNL ..... ±0.3 LSB typ, ±0.75 LSB max

Spurious free dynamic range

Gains 0.2-0.5 ..... 70 dB, DC to 100 kHz

Gains 1-50 ..... 75 dB, DC to 100 kHz

Effective number of bits (ENOB)..... 11.0 bits, DC to 100 kHz

Offset error

| Gain | Gain Error[1] | Offset Error |
|---|---|---|
| 0.2 | 0.50% | 10 mV |
| 0.5 | 0.50% | 10 mV |
| 1 | 0.10% | 0.8 mV |
| 2 | 0.05% | 0.5 mV |
| 5 | 0.05% | 0.28 mV |
| 10 | 0.05% | 0.20 mV |
| 20 | 0.05% | 0.15 mV |
| 50 | 0.05% | 0.10 mV |
| [1] Relative to reading, max | | |

## Amplifier Characteristics

Input impedance ..... 1 MΩ in parallel with 100 pF

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR, all input ranges, DC to 60 Hz

| Gain | CMRR |
|---|---|
| 0.2 | 32 dB |
| 0.5 | 35 dB |
| 1.0 | 50 dB |
| 2.0 | 56 dB |
| 5.0 | 62 dB |
| 10.0 | 67 dB |
| 20.0 | 70 dB |
| 50.0 | 72 dB |

## Dynamic Characteristics

Bandwidth .....5 MHz

System noise (LSBrms, not including quantization)

| Gain | Noise |
|---|---|
| 0.2 to 10 | 0.5 |
| 20 | 0.6 |
| 50 | 1.0 |

Crosstalk.....–80 dB, DC to 100 kHz

## Stability

Recommended warm-up time.....15 min.

Offset temperature coefficient

Pregain.....±5 µV/° C

Postgain .....±50 µV/° C

Gain temperature coefficient.....±20 ppm/° C

Onboard calibration reference

Level.....5.000 V (±2.5 mV) (actual value stored in EEPROM)

Temperature coefficient..... ±0.6 ppm/° C max
Long-term stability..... ±6 ppm/ $\sqrt{1,000\ h}$

# Analog Output

## Output Characteristics

Number of channels ..... 2 voltage

Resolution..... 16 bits, 1 in 65,536

Max update rate
- 1 channel..... 4 MS/s, system dependent
- 2 channel..... 2.5 MS/s, system dependent

FIFO buffer size..... 8,192 samples

Data transfers..... DMA, interrupts, programmed I/O

DMA modes..... Scatter-gather

## Transfer Characteristics

Relative accuracy (INL)..... ±4 LSB typ, ±8 LSB max

DNL..... ±2 LSB typ, ±8 LSB max

Offset error ..... ±5.0 mV max

Gain error
(relative to internal reference)..... ±0.1% of output range max

## Voltage Output

Ranges ..... ±10 V

Output coupling ..... DC

Output impedance ..... 50 Ω ±5%

Current drive..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state..... 0 V

## Dynamic Characteristics

Slew rate.....300 V/µs

Noise .....1 $mV_{rms}$, DC to 5 MHz

Spurious free dynamic range.....75 dB, DC to 10 kHz

## Stability

Offset temperature coefficient.....±500 µV/° C

Gain temperature coefficient

Internal reference .....±50 ppm/° C

External reference .....±25 ppm/° C

Onboard calibration reference

Level.....5.000 V (±2.5 mV) (actual value stored in EEPROM)

Temperature coefficient .....±0.6 ppm/° C max

Long-term stability.....±6 ppm/ $\sqrt{1,\ 000\ h}$

# Digital I/O

Number of channels.....8 input/output

Compatibility.....TTL/CMOS

Digital logic levels

| Level | Min | Max |
|---|---|---|
| Input low voltage | 0.0 V | 0.8 V |
| Input high voltage | 2.0 V | 5.0 V |
| Input low current ($V_{in}$ = 0 V) | — | –320 µA |
| Input high current ($V_{in}$ = 5 V) | — | 10 µA |
| Output low voltage ($I_{OL}$ = 24 mA) | — | 0.4 V |
| Output high voltage ($I_{OH}$ = 13 mA) | 4.35 V | — |

Power-on state .....Input (High-Z)

Data transfers.....Programmed I/O

# Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns, edge-detect mode

Min gate pulse duration ..... 10 ns, edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather

# Triggers

## Analog Trigger

Source

- PCI-6110E ..... ACH<0..3>, external trigger (PFI0/TRIG1)
- PCI-6111E ..... ACH<0..1>, external trigger (PFI0/TRIG1)

Level ..... ± full-scale, internal; ±10 V, external

Slope ..... Positive or negative (software selectable)

Resolution ..... 8 bits, 1 in 256

Hysteresis ..... Programmable

Bandwidth (–3 dB) ..... 5 MHz internal/external

External input (PFI0/TRIG1)

Impedance ..... 10 kΩ

Coupling ..... AC/DC

Protection ..... –0.5 V to ($V_{cc}$ + 0.5) V when configured as a digital signal, ±35 V when configured as an analog trigger signal or disabled, ±35 V powered off

## Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width ..... 10 ns min

## RTSI

Trigger Lines ..... 7

## Bus Interface

Type ..... Master, slave

## Power Requirement

+5 VDC (±5%)

PCI-6110E ..... 2.5 A

PCI-6111E ..... 2.0 A

Power available at I/O connector ..... +4.65 to +5.25 VDC at 1 A

## Physical

Dimensions
(not including connectors) ..... 31.2 by 10.6 cm (12.3 by 4.2 in)

I/O connector ..... 68-pin male SCSI-II type

## Environment

Operating temperature ..... 0° to 55° C

Storage temperature ..... –55° to 150° C

Relative humidity ..... 5% to 90% noncondensing